A *K*/*Ka*-Band Distributed Power Amplifier with Capacitive Drain Coupling

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Abstract—**A 14 to 37 GHz GaAs MMIC distributed power amplifier has been demonstrated. The amplifier has three FET's of varying periphery, all capacitively coupled to the gate line. A new circuit concept has been used to increase output power: the drain of the FET nearest the output is capacitively coupled to the drain line. A gain of 4 to 5 dB has been achieved from 14 to 37 GHz. Output power of 20 dBm or greater has been demonstrated at frequencies up to 33 GHz at 1 dB gain compression. A maximum 1 dB gain-compressed output power of 23.5 dBm (220 mW) has been measured at 26 GHz. The circuit is completely monolithic, with all bias and matching circuitry included on the chip.**

I. Introduction

DISTRIBUTED amplifiers offer a means of achieving gain at high frequencies and over wide bandwidths by incorporating active device parasitic capacitances into artificial transmission lines [1]. This technique has successfully been applied to GaAs MMIC's with MESFET gain elements. It has been shown that the combination of gate capacitance and gate resistance causes attenuation along the gate artificial transmission line (the gate line), effectively limiting total gate periphery and amplifier gain [2].

Distributed amplifiers operating up to *Ka*-band have been demonstrated with output power levels of 12 to 15 dBm [3], [4]. Varying FET size can be utilized to increase total FET periphery, resulting in modest improvements in gain and output power [3].

At lower frequencies it has been demonstrated that capacitively coupling FET gates to the gate line allows the total FET periphery to be increased dramatically, resulting in higher output power without a significant change in gain [5]. The gate coupling capacitors are in series with the FET gate, and reduce the effective gate capacitance of the gate line. Periphery can then be increased to the point where effective gate capacitance reaches its original level. The gate coupling capacitors reduce the voltage at the gate of each FET, but this is compensated for by the increased periphery, and gain essentially remains unchanged. Higher output power is possible because more drain current is available from the larger total FET periphery, and because the RF voltage level at the gate is reduced, which forestalls gate voltage limiting.

The use of gate coupling capacitors allows the total FET periphery to be dramatically increased over a conventional distributed amplifier. With much higher total FET periphery, new effects limit the performance of the amplifier. Drain line loading begins to limit output power, particularly at the upper end of the operating band. The resulting output power cutoff is lower in frequency than the small-signal gain cutoff.

II. Circuit Design Considerations and Example

In a conventional distributed amplifier, performance limitations are dominated by gate effects; drain effects are secondary. This may be attributed to the relative value of the gate capacitance. Gate capacitance (C_{gs}) is typically 2 to 4 times drain capacitance (C_{ds}). The use of gate coupling capacitors allows a FET periphery to be increased, without increasing the effective gate capacitance seen by the gate line [5]. The drain line continues to be directly coupled to the FET's, however, and must accommodate the increased periphery. Analysis of the drain line shows that drain line loading significantly limits the performance of the amplifiers, particularly in output power at the high end of the band.

Insight into the effects of drain line loading may be gained by calculating the impedance at the drain nodes of the FET's. This impedance is calculated as the ratio of the voltage at the drain node to the current through the node, with all FET's connected and active. When drain line loading occurs, the real part of the impedance at the drains of the FET's nearest the output become very low and sometimes even negative at the upper end of the operating band. When the real part of the impedance is low, the FET contributes very little to the total output power. When the real part of the impedance is negative, the FET is absorbing more RF power than it generates. The low impedances imply that the FET's are driving little power into a load, and amplifier output power is limited.

Once drain line loading begins to limit output power, significantly higher output power cannot be achieved by changing periphery. Further increasing the total FET periphery increases the output current capacity of the FET's, but it also causes the real part of the impedance at the drain to decrease, and total output power does not in-

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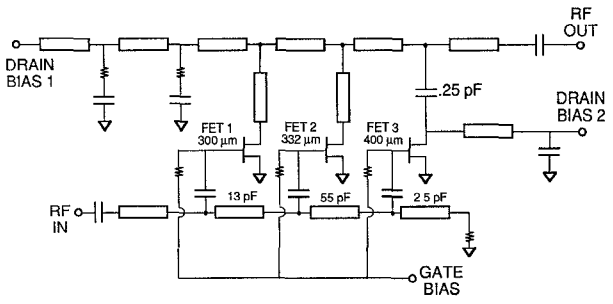


Fig. 1. Schematic of a distributed amplifier with the drain of FET3 capacitively coupled to the drain line.

crease. Drain line loading may be avoided by reducing the periphery, but FET output current capacity is also reduced, and total output power does not improve.

A new technique has been devised to increase output power. A capacitor is inserted between the drain line and the drain of any FET with a low or negative real part of the impedance. This decreases drain line loading and increases the impedance at the drains. Higher total FET periphery can be accommodated; thus, higher output power may be achieved.

An example of a distributed amplifier using capacitive drain coupling is shown in Fig. 1. This circuit, which operates from 14 to 37 GHz, also features varying gate periphery and capacitive gate coupling. The total FET periphery is 1.03 mm. A drain coupling capacitor is used at FET3. Analysis of this circuit will be used to demonstrate the effectiveness of the drain coupling capacitor. It is shown below, in Section IV, that the analysis used adequately predicts both the gain and the output power of the amplifier.

The amplifier was analyzed for small-signal performance using a conventional commercial linear microwave design program. In addition to gain calculations, relative RF voltages and currents were calculated at various nodes of the circuit. These nodes include the amplifier input and output, each FET gate, and each FET drain. Knowing the limitations of the device (pinch-off voltage, breakdown voltage, I_{dss}, knee voltage), it is possible to determine when an output power limit is reached, and which device limitation is the cause. It has been found that this power limit calculation correlates well with measured power output at 1 dB compression.

This analysis also allows the impedance at each drain to be calculated (from the node voltage and current). When the real part of the impedance seen at any drain node is low, very little RF power is being contributed by that FET. When the real part of this calculated impedance is negative, the FET is absorbing more power than it generates.

The impedance at the drain of each of the three FET's has been calculated with the drain of FET3 coupled to the drain line both directly and through the 0.25 pF capacitor. The real parts of these impedances are plotted in Fig. 2. Without the capacitor at drain 3, the real part of impedance is very low (less than 5 Ω) at frequencies above 23

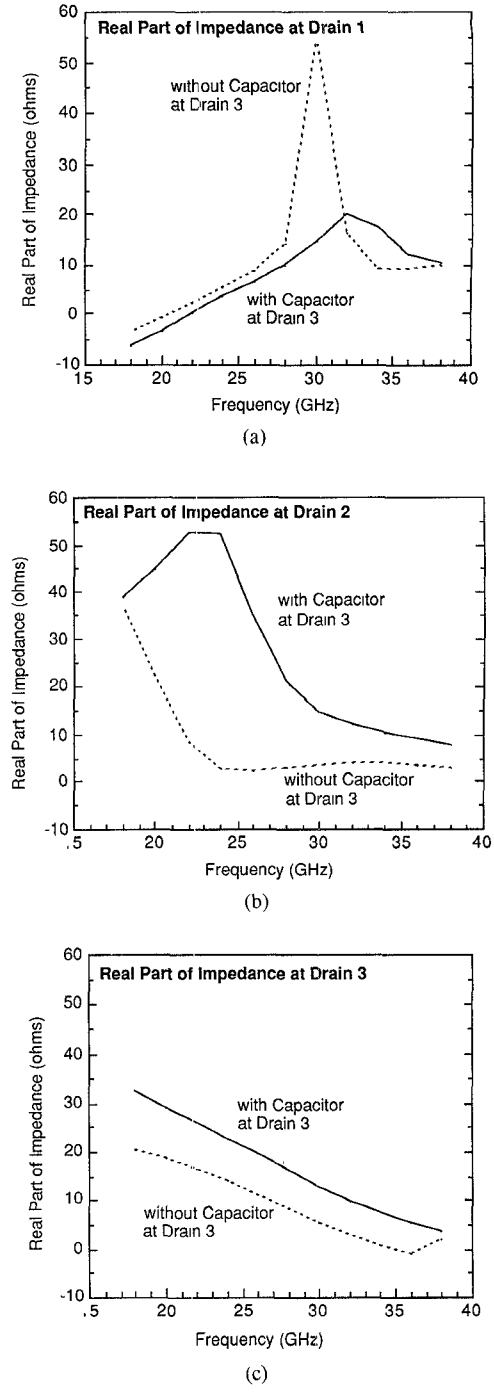


Fig. 2. Real part of the impedance with and without the FET3 drain coupling capacitor at (a) the drain of FET1, (b) the drain of FET2, and (c) the drain of FET3.

GHz for FET2, and at frequencies above 29 GHz for FET3. Because of these low impedances, the drain currents of these FET's severely limit the output power of the amplifier.

The plots in Fig. 2 show the improvement in the real parts of the drain impedances with the insertion of the FET3 drain coupling capacitor. The reactive parts of the drain impedances are also affected, but the changes are relatively small, and do not have a dramatic effect on amplifier performance. As is the case for most distributed

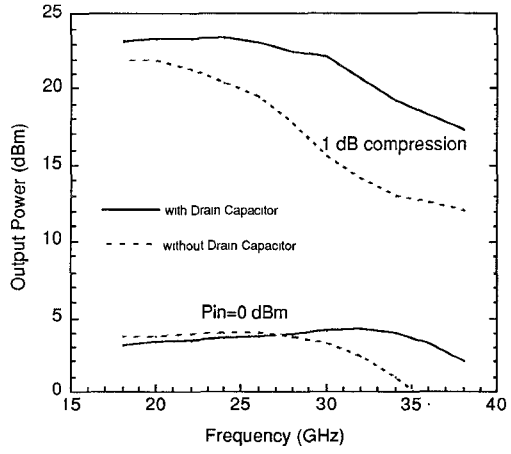


Fig. 3. Predicted gain and 1 dB gain compressed power for the amplifier with and without the FET3 drain coupling capacitor.

amplifiers, the drain impedances are actually quite far from optimal power match conditions. By inserting the capacitor at the drain of FET3, the drain impedances move nearer the optimal power match condition, primarily by increasing the resistive part of the load.

As can be seen in Fig. 2, inserting the 0.25 pF capacitor between FET3 and the drain line substantially increases the real part of the impedances at the drains of FET2 and FET3 over the 18–38 GHz frequency range. Since amplifier output power is primarily limited by the drain current of these FET's, substantially higher amplifier output power is realized. The real part of the impedance at drain 1 is also altered, but does not play a significant role in power limiting.

The gain and power performance of the circuit in Fig. 1 have been modeled both with and without the 0.25 pF capacitor in place between drain 3 and the drain line. The results are plotted in Fig. 3. Gain is represented as output power with a 0 dBm input. The addition of the capacitor reduces gain slightly at lower frequencies but extends flat gain to substantially higher frequencies. The insertion of the FET3 drain coupling capacitor also forestalls power limitations, as was expected from Fig. 2. At 18 GHz the output power increases by 1.5 dB, and at 27 GHz by 5 dB. The insertion of the capacitor between the drain of FET3 and the drain line provides for higher, flatter power performance to much higher frequencies. In this case the amplifier provides 20 dBm up to 25 GHz without the capacitor, up to 33 GHz with the capacitor.

Normally the drains of all FET's are biased through the drain line. The addition of the drain coupling capacitor prevents FET3 from being biased in the normal way. Instead, a separate drain bias network is used for FET3, comprising a large value capacitor and a quarter-wave transformer. It is important that the bias network present a very high impedance in order to avoid degrading amplifier performance. The transformer is a quarter wavelength long near the band center, but presents a sufficiently high impedance over the entire 15 to 37 GHz frequency band. In the modeling that was done for Figs. 2 and 3, the transformer was included in the amplifier model only when the capacitor was inserted between the drain of FET3 and the drain line.

III. Circuit Fabrication

The completed circuit is shown in Fig. 4. The circuit is fully monolithic; all bias circuitry is included on the chip. Each gate is biased from a common node through 2 kΩ resistors consisting of multiple open-gate FET's. Two drain biases are provided. The first is a low-pass filter and connects to FET1 and FET2; the second connects to FET3 and consists of a quarter-wave transformer and a large capacitor. RF input and output are dc isolated.

MBE material was used with an active layer carrier concentration of 4.5×10^{17} cm^{-3} and a contact layer concentration of 3×10^{18} cm^{-3}. The FET's have 0.25 μm, e-beam defined gates. Fig. 5 shows the FET model and the element values that were used. Silicon nitride with a thickness of 0.2 μm was used both as a capacitor dielectric and as passivation. The substrate was thinned to 100 μm, and 20 × 100 μm via holes were plasma etched. The complete chip measures 54 × 82 mils (1.4 × 2.1 mm).

IV. Circuit Performance

Measured data for two amplifiers are presented in this paper; amplifier #1 uses low-current devices, amplifier #2 uses high-current devices. Otherwise the amplifiers are identical. The combined I–V curves for all the FET's in amplifier #1 (1.03 mm total periphery) are shown in Fig. 6. The measured small-signal performance of the amplifier is shown in Fig. 7. Flat 4–5 dB gain has been achieved from 14 to 37 GHz with the FET's biased at I_{dss}. Input return loss is better than 10 dB at the bottom of the band, but gradually degrades to 6 dB at the top of the band. Output return loss is better than 10 dB except at the bottom of the band, where it is 8 dB.

Power performance for amplifier #1 was measured under the same bias conditions as small-signal performance (I_{dss}), and is summarized in Fig. 8. Output power curves are shown for various input power levels as well as at 1 dB and 1.5 dB gain compression. A curve for a 0 dBm input power is included for convenient verification of small-signal performance. At 1 dB gain compression, output power is better than 19 dBm up to 34 GHz. At 1.5 dB gain compression, output power is better than 20 dBm up to 34 GHz, and better than 19 dBm to 35 GHz.

The I–V curves for amplifier #2 are shown in Fig. 9. The devices in this amplifier have nearly twice the I_{dss} of those in amplifier #1. The small-signal gain and the power performance of amplifier #2 are shown in Fig. 10. An output power of better than 20 dBm has been achieved to 33 GHz at 1 dB gain compression. A maximum 1 dB gain-compressed power of 23.5 dBm (220 mW) has been achieved at 26 GHz. The small-signal gain of this chip is indicated by the $P_{in} = 0$ dBm curve at the bottom of Fig. 10. Amplifier #2 has considerably higher output power and slightly lower gain than amplifier #1.

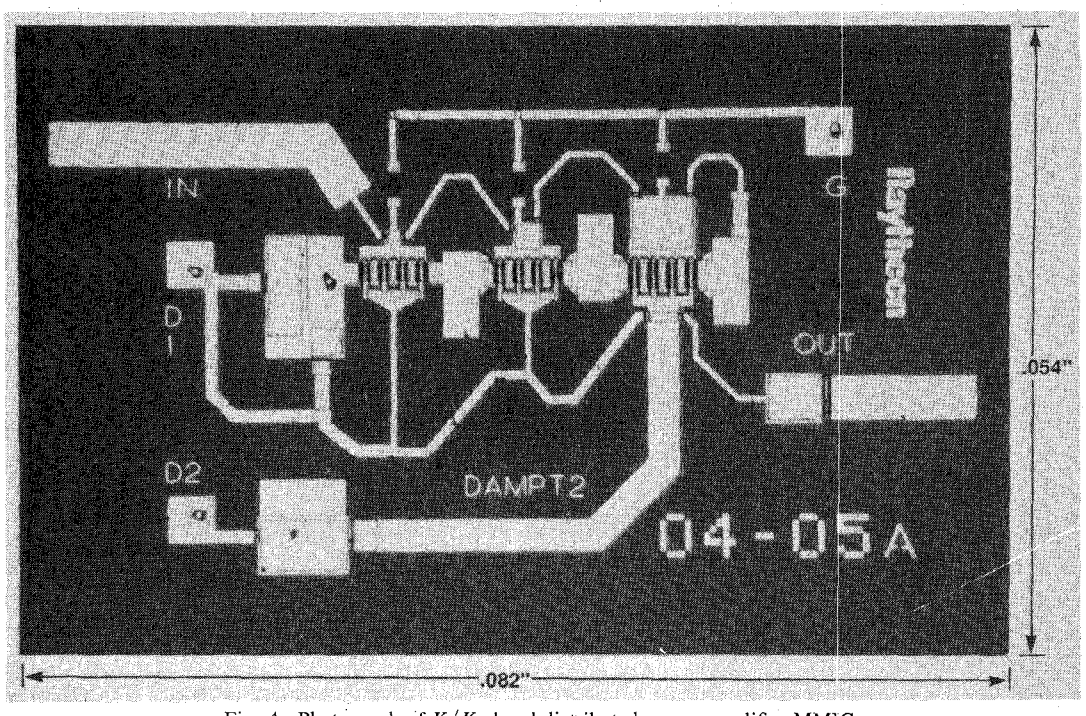
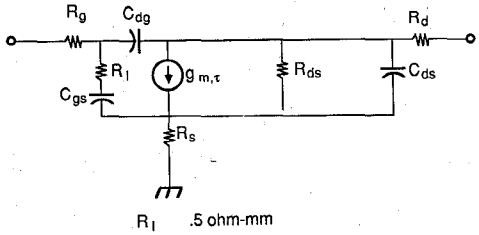


Fig. 4. Photograph of *K/Ka*-band distributed power amplifier MMIC.



R_I	.5 ohm-mm
C_{gs}	.85 pF-mm^{-1}
g_m	240 mS-mm^{-1}
τ	1.0 psec
G_{ds}	27 mS-mm^{-1}
C_{ds}	.35 pF-mm^{-1}
C_{dg}	.12 pF-mm^{-1}
R_g	.35 ohm-mm
R_s	.22 ohm-mm
R_d	.22 ohm-mm

Fig. 5. FET model with element values.

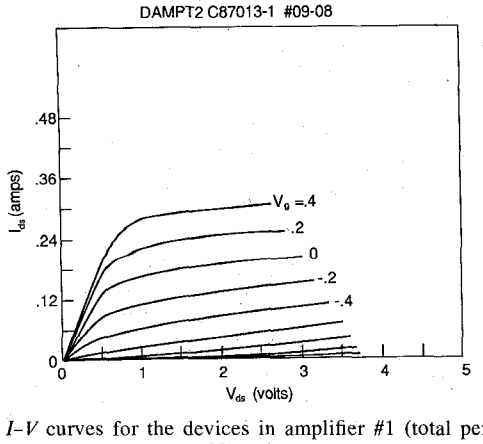


Fig. 6. dc *I–V* curves for the devices in amplifier #1 (total periphery is 1.03 mm).

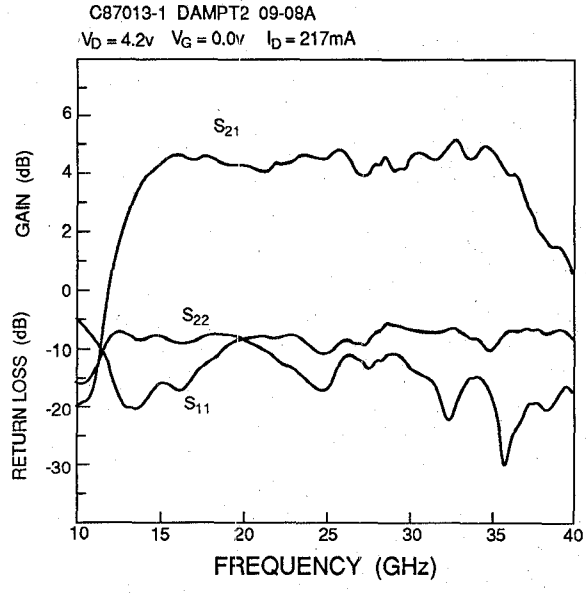


Fig. 7. Small-signal performance of amplifier #1.

The performance of amplifier #2 has been modeled using the methods described in Section II above. Measured and modeled performances are compared in Fig. 11. The measured performance shown in Fig. 11 is the same as that shown in Fig. 10. Both measured gain and 1 dB gain-compressed output power have been predicted within 1 dB of the measured performance from 20 to 36 GHz. FET performance limitations used in modeling the output power of the amplifier are taken from the *I–V* curves in Fig. 9. The model shows that power is limited by the voltage swing at the gate of FET3 from 15 to 26 GHz, by the drain current of FET2 from 26 to 30 GHz, and by the drain current of FET3 above 30 GHz.

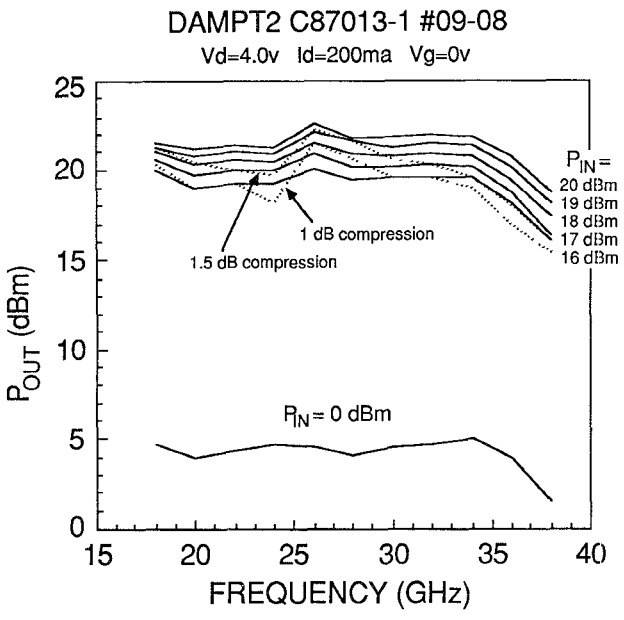


Fig. 8. Power performance of amplifier #1. Small-signal performance is included as the P_{in} = 0 dBm curve.

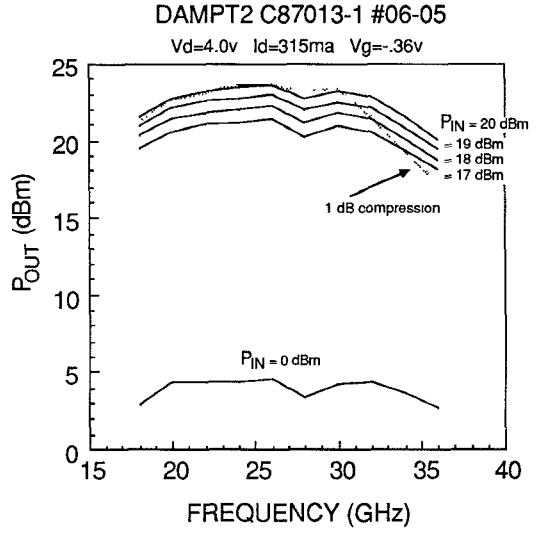


Fig. 10. Power performance of amplifier #2. Small-signal performance is included as the P_{in} = 0 dBm curve.

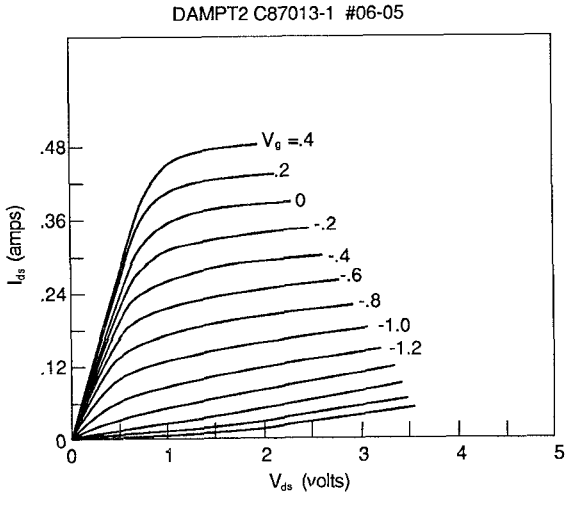


Fig. 9. dc *I–V* curves for the devices in amplifier #2 (total periphery is 1.03 mm).

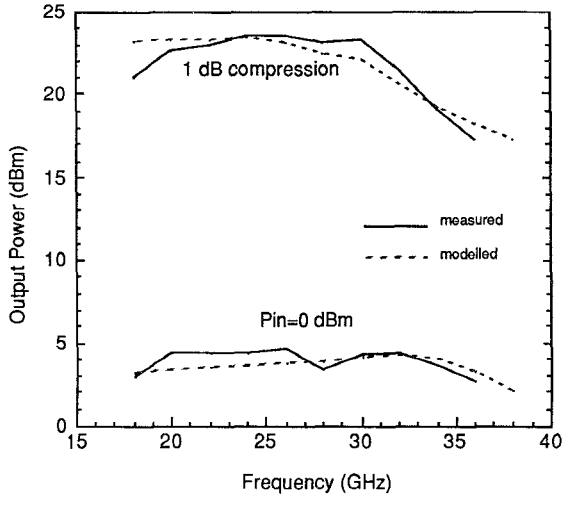


Fig. 11. Comparison of modeled and measured performance for the *K/Ka*-band distributed power amplifier.

V. Summary

A *K/Ka*-band distributed power amplifier has been demonstrated in MMIC form. It incorporates a novel circuit feature, capacitive drain coupling. The drain coupling capacitor reduces drain line loading, increasing the real part of the impedance seen at the drains of the FET's, and results in higher output power. More than 100 mW has been achieved up to 34 GHz. A maximum 1 dB gain-compressed output power of 220 mW has been demonstrated at 26 GHz. Both output power and small-signal gain have been modeled within 1 dB of the measured values.

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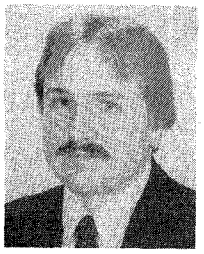

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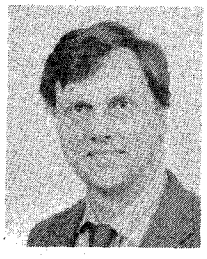

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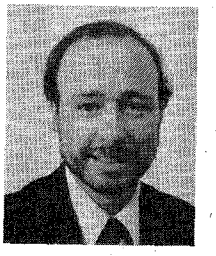

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